



#61 Amdt B
4/13/03
C.P.

PATENTS

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): Bijan Davari, et al.

Examiner: Long Pham

Serial No.: 09/975,435

Art Unit: 2814

Filed: October 11, 2001

Docket: YOR919990101US2 (16322)

For: PATTERNED SOI REGIONS ON
SEMICONDUCTOR CHIPS

Dated: April 14, 2003 (Mon)

Commissioner for Patents
Washington, DC 20231

AMENDMENT AND RESPONSE

Sir:

In response to the Office Action dated November 13, 2002, applicants submit the following amendments and remarks for entry of record in the above-identified patent application.

IN THE CLAIMS:

Please amend Claims 35, 53 and 55 to read as follows:

35. (Amended) A method for forming spaced apart silicon-on-insulator (SOI) regions in an upper region of a silicon containing substrate comprising the steps of:

CERTIFICATE OF MAILING UNDER 37 C.F.R. §1.8(a)

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, D.C. 20231 on April 14, 2003 (Mon).

Dated: April 14, 2003 (Mon)

Mishelle Mustafa

RECEIVED
APR 21 2003
TECHNOLOGY CENTER